UNIVERSITY OF SOUTH FLORIDA

Defense of a Master's Thesis

Threshold Voltage Defined Switches and Gates to Prevent Reverse Engineering

by

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For the MSCP degree in Computer Science & Engineering

Semiconductor supply chain is increasingly getting exposed to variety of security attacks such as Trojan insertion, cloning, counterfeiting, Reverse Engineering (RE), piracy of Intellectual Property (IP) or Integrated Circuit (IC) and side-channel analysis due to involvement of untrusted parties. We propose threshold voltage-defined switches that will camouflage the logic gate both logically and physically to resist RE and IP piracy. The proposed gate can function as NAND, AND, NOR, OR, XOR, and XNOR robustly using threshold defined switches. We also propose a flavor of camouflaged gate that represents reduced functionality (NAND, NOR and NOT) at much lower overhead. The camouflaged design operates at nominal voltage and obeys conventional reliability limits. A small fraction of gates can be camouflaged to make the RE effort extremely high. A significant higher RE effort is achieved when the proposed gate is employed in the netlist using controllability, observability and hamming distance sensitivity based gate selection metrics.

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1:00pm-2:00pm
ENB 313

THE PUBLIC IS INVITED

Examining Committee

Dr. Srinivas Katkoori, Ph.D., Major Professor
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