UNIVERSITY OF SOUTH FLORIDA

Defense of a Master's Thesis

Novel Bit-sliced In-memory Computing Based VLSI Architecture for Fast Sobel Edge Detection in IoT Edge Devices

by

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For the MSCP degree in Computer Science & Engineering

For today's Internet-of-Things (IoT) edge devices, there is an acute need for fast and power efficient hardware for image processing task. Traditional hardware solutions with sequential and/or pipelined architectures incur high latency and power. This motivates us to propose a novel in-memory computing architecture for rapid image processing. We propose a bit-sliced in-memory computing architecture for CMOS VLSI implementation for fast Sobel edge detection. To the best of our knowledge, this is the first work to propose an in-memory computing based VLSI architecture for the edge detection. The novelty of the proposed work is that one image can be processed in constant time irrespective of the image size. Binary images are used as an input to the design. The Sobel operator equations are simplified by operator strength reduction, bit manipulation, and common term sharing across equations. The captured image is loaded into the design and all block level operations are executed in parallel close to where the data resides. The architecture is highly modular and can be scaled for any image size. The block processing element (PE) is implemented at the layout-level with Synopsys tool suite. For processing one block frame (3 x 3 pixel block), the number of logic gates is 17 with a worst-case delay of 3.52 fs and total bounding box layout area of 158 nm^2. The estimated average power dissipation is 0.72 μW at 0.7 V supply voltage.

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12:00 pm
ENB 337

THE PUBLIC IS INVITED

Examining Committee

Srinivas Katkoori, Ph.D., Major Professor
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Mehran Mozaffari Kermani, Ph.D.

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