UNIVERSITY OF SOUTH FLORIDA

Defense of a Master's Thesis

Voltage droop analysis and mitigation in a STTRAM Last Level Cache

by

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For the MSCS degree in Computer Science & Engineering

Spin-Transfer Torque Random Access Memory (STT-RAM) is one of the emerging Non-Volatile Memory (NVM) technologies especially preferred for a Last Level Cache (LLC). The amount of current needed to switch the magnetization is high (~100μA per bit). For a full cache line (512-bit) write, this extremely high current results in a voltage droop in the conventional cache architecture. Due to this droop, the write operation fails especially when the farthest bank of the cache is accessed. In this Thesis, we do an analysis of the voltage droop across the STT RAM LLC and then propose a new cache micro-architecture to mitigate this problem and make the write operation successful. Instead of continuously writing the entire cache line (512-bit) in a single bank, the proposed architecture writes 64-bits in multiple physically separated locations across the cache. The simulation results obtained (both circuit and micro-architectural) comparing our proposed architecture against the conventional are found to be 1.96% (IPC) and 5.21% (energy).

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THE PUBLIC IS INVITED

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