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presents

Leveraging Tunable Randomness in Spin-based Devices for Neuromorphic and Secure Computation Computing

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Abstract: Recent research in emerging device technologies for computing seeks to advance: (1) novel processor architectures embracing paradigms such as processing-in-memory and neuromorphic computation, (2) innovative circuit solutions to CMOS scaling challenges of area and leakage power, and (3) the ability to impart unique security attributes. An approach spanning all three of these goals is identified for spintronic devices such as Magnetic Tunnel Junctions (MTJs), which are identified on the ITRS Roadmap as promising complementary devices for MOSFETs due to their non-volatility, near-zero standby power, vertical integration at the back-end-of-line of CMOS fabrication, and their commercial availability as non-volatile secondary memory and tertiary storage. This talk will explore two domains of future hybrid MTJ/MOS computing using a unique design perspective. Namely, the advantages of each device technology are leveraged by embracing tunable randomness of spin-based devices to advance neuromorphic operations in-situ and hardware security at low device count, alongside of traditional deterministic logic functions at which CMOS excels. A hybrid spin/CMOS based low-energy hardware implementation of a Deep Belief Network (DBN) architecture will be presented that utilizes near-zero energy barrier probabilistic spin logic devices, which are modeled to intrinsically compute a sigmoidal activation with tunable randomness. Next, the Non-Volatility (NV) feature of spin-based devices will be discussed towards the objectives of advancing secure, intermittency-tolerant, and energy-aware logic datapaths by developing a design methodology and its corresponding synthesis steps. Together these advance new circuit and architectural approaches to realizing neuromorphic computation and dependability through the targeted utilization of post-CMOS emerging devices.

Bio: Ronald F. DeMara received the Ph.D. degree in Computer Engineering from the University of Southern California in 1992. Since 1993, he has been a full-time faculty member at the University of Central Florida where he is a Professor of Electrical and Computer Engineering, and joint faculty of Computer Science, and has served as Associate Chair, ECE Graduate Coordinator, and Computer Engineering Program Coordinator. His research interests are in adaptive computer architectures with emphasis on reconfigurable and post-CMOS devices, evolvable and intelligent hardware, resilient and energy-aware logic design, and the digitization of STEM education. On these topics, he has completed over 250 publications, 47 funded projects as PI or Co-PI including sponsorship of NSF, NASA, Army, Navy, Air Force, DARPA, and NSA, with one patent granted and one provisional patent. He has completed 44 graduates as Ph.D. dissertation or M.S. thesis advisor and was previously an Associate Engineer at IBM and a Research Scientist at NASA Ames, in total for four years. He is a Senior/Topical Editor of IEEE Transactions on Computers and has served on the Editorial Boards of IEEE Transactions on VLSI Systems, Microprocessors and Microsystems, and as Guest Editor of various Transactions, and serves on various IEEE conference program committees including ISVLSI, NVMSA, SSCI, etc. He received the IEEE Joseph M. Bidenbach Outstanding Engineering Educator Award in 2008.