UNIVERSITY OF SOUTH FLORIDA

Major Research Area Paper Presentation

High Level Synthesis Techniques for Secure Hardware Design

by

Sheikh Ariful Islam

For the Ph.D. degree in Computer Science & Engineering

Stringent time-to-market requirement for reduced design cycle time has increased manufacturing complexity and fabrication cost of miniaturized electronics devices. Outsourcing designs and inclusion of untrustworthy third-party intellectual property (3PIP) cores are dominant in integrated circuit (IC) design flow. It is likely for any or multiple parties involved in horizontal IC business model to be untrustworthy. The effect of such adversary can be multifold. Techniques to protect hardware during post-synthesis are already in practice, there is less effort to secure hardware units built upon a particular algorithmic description during pre-synthesis. High Level Synthesis (HLS) is the process of transforming an algorithm into an RT level design. To build a resilient system against internal and external attacks, HLS techniques can help during early stage of design cycle. In this presentation, we will review existing HLS techniques to provide countermeasures against hardware attacks.

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THE PUBLIC IS INVITED

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