UNIVERSITY OF SOUTH FLORIDA

Defense of a Master's Thesis

Gate Level Probabilistic Simulation Based Hardware Trojan Susceptibility Analysis of Combinational Circuits

by

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For the MSCS degree in Computer Science & Engineering

Today multi-million gate integrated circuits are being commonly used in many critical (eg., health care) and sensitive (eg., military) applications. Therefore, they are susceptible to malicious modifications, namely, Hardware Trojans (HTs), with the intent of leaking sensitive information, denial-of-service etc. There are many ways of inserting Hardware Trojans in ICs. Thus, HT detection and mitigation are very important tasks. In this thesis, we propose a novel probabilistic simulation based approach to estimate the susceptibility of a combinational circuit to a HT. One of the common ways is to simulate the netlist with typical input sequences and identifying low activity nets in the design that could be exploited for Hardware Trojans. This approach has the drawback of excessive simulation time. Probabilistic simulation is very efficient as the input sequences are condensed into probabilistic waveforms which are then propagated through the netlist to identify low activity nets. The main advantage of the proposed technique is rapid analysis of a netlist for HT susceptibility. We experimented with MCNC benchmark suite and demonstrate significant speedup over traditional simulation based approach.

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THE PUBLIC IS INVITED

Examining Committee

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