UNIVERSITY OF SOUTH FLORIDA

Major Research Area Paper Presentation

A System Level Protocol Guided Solution for Post-Silicon System-on-Chip Debug
by
Yuting Cao

For the Ph.D. degree in Computer Science & Engineering

Post-silicon debug is a critical component of the design validation life-cycle for modern microprocessors and System-on-Chip (SoC) designs. Unfortunately, it is also highly complex, performed under aggressive schedules and accounting for more than 50% of the overall design validation cost. Due to the complexity and high concurrency of the modern SoC, the communication activities become the major source of complexity during SoC execution. Therefore, it is beneficial to focus on construct a system-level behavior from the system level communication activities. This presentation provides an overview of current post-silicon validation status, existing challenges and possible solutions. Furthermore, it discusses various features that can be enhanced to enable system level validation for post-silicon SoC debug.

02/13/2018
10:00 am
ENB 313

THE PUBLIC IS INVITED

Examining Committee
Hao Zheng, Ph.D., Major Professor
Swaroop Ghosh, Ph.D.
Srinivas Katkoori, Ph.D.
Sandip Ray, Ph.D.
Sanjukta Bhanja, Ph.D.

Miguel Labrador, Ph.D.
Graduate Program Director
Computer Science and Engineering
College of Engineering

Sudeep Sarkar, Ph.D.
Department Chair
Computer Science and Engineering
College of Engineering